REMARKS

Claims 7-22 are pending in this application. By this Amendment, claims 7 and 8 are amended. No new matter is added. The specification provides support for the amended claims.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (as the amendments merely delete prior claim language); (c) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

I. Rejection Under 35 U.S.C. §103(a)

Claims 7-22 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,362,076 (hereinafter Inazuki) in view of U.S. Patent 6,544,656 (hereinafter Abe)*. This rejection is respectfully traversed.

Claim 7 recites a method of producing an SOI wafer comprising at least the steps of forming an insulator film on at least one of a bond wafer made of silicon single crystal to form an SOI layer and a base wafer made of silicon single crystal to be a support substrate, bonding each main surface of the bond wafer and the base wafer via the insulator film, and

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* Applicant notes that U.S. Patent No. 6,544,656 cannot be cited against the claims under 35 U.S.C. §103(a). This patent is owned by Shin-Etsu Handotai Co., Ltd., the same assignee as the present application, and is prior art under only 35 U.S.C. §102(e) (see MPEP §706.02(f)(1), Example 6). Thus, under 35 U.S.C. §103(c), U.S. Patent No. 6,544,656 is not citable under 35 U.S.C. §103(a). However, the corresponding PCT application of U.S. Patent No. 6,544,656 (WO 00/55397) appears to be available under 35 U.S.C. §102(b), and thus the teachings of Abe are addressed herein on the merits.

making the bond wafer bonded to the base wafer thinner, wherein the base wafer is one silicon wafer selected from a group consisting of an epitaxial wafer, a nitrogen doped wafer, a hydrogen annealed wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer.

Claim 8 recites a method of producing an SOI wafer comprising at least the steps of forming an insulator film on at least one of a bond wafer made of silicon single crystal to form an SOI layer and a base wafer made of silicon single crystal to be a support substrate, forming a micro bubble layer in the bond wafer by implanting gas ions from a main surface of the bond wafer, bonding the ion-implanted main surface of the bond wafer to a main surface of the base wafer via the insulator film, and delaminating the bonded wafer at the micro bubble layer as a border, wherein the base wafer is one silicon wafer selected from a group consisting of an epitaxial wafer, a nitrogen doped wafer, a hydrogen annealed wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer.

Therefore, independent claims 7 and 8 of the present application relate to methods of producing an SOI wafer using a bond wafer made of silicon single crystal to form an SOI layer and a base wafer made of silicon single crystal to be a support substrate. A main feature of the methods is that one silicon wafer selected from a group consisting of an epitaxial wafer, a nitrogen doped wafer, a hydrogen annealed wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer is used as the base wafer.

As disclosed in the specification, Applicant observed that crystal originated particles (COPs) did not exist in the SOI layer, but existed on a surface of a base wafer serving as a support substrate, as shown in Fig. 4. Namely, it became clear that since the SOI layer and the insulator film were made thin, COPs existing in the base wafer had been detected as COPs existing in the SOI layer (see page 6, lines 15-22 of the specification). Moreover, as shown in Fig. 5, the insulator film and the base wafer could not be bonded in the region in which the COPs existed, thus resulting in a micro void (see page 7, lines 1-13 of the

specification). However, when a SOI wafer is produced by using an epitaxial wafer and the like as the base wafer, measurements which precisely reflect the number of COPs in the SOI layer can be performed. Thus, when the SOI wafer is produced by bonding the bond wafer to the base wafer via the insulator film and thinning the bond wafer, if an epitaxial wafer and the like is used as the base wafer, an SOI wafer that COPs hardly exist near a surface of the base wafer can be obtained. Also, a high quality SOI wafer in which generation of micro voids at an interface between the base wafer and the insulator film is suppressed can be produced (see page 8, lines 3-21 of the specification).

The Patent Office initially asserts that Inazuki discloses the use of an epitaxial wafer or an FZ wafer as the base wafer as recited in claims 7 and 8. Applicant disagrees.

Inazuki discloses a method of fabricating an SOI wafer by the hydrogen ion delamination method using a base wafer 1 and a bond wafer 2 (see Fig. 1 and col. 4, lines 46-56). Inazuki only describes that a silicon mirror polished wafer is used as the base wafer and never teaches or suggests using an epitaxial wafer or the like as a base wafer (see col. 4, lines 45-51). In Figure 1, Inazuki discloses the steps of fabricating an SOI wafer and only include the heat treatment conditions and the bonding heat treatment (f) of Fig. 1. Inazuki merely states that when the bond wafer is an epitaxial wafer or an FZ wafer, the buried oxide layer is not reduced (see col. 6, lines 39-45). As such, Inazuki neither teaches nor suggests the use of an epitaxial wafer or the like as a base wafer. Inazuki does not teach or suggest use of a silicon wafer wherein COPs hardly exist near its surface including an epitaxial wafer and the like as a base wafer.

Moreover, the base wafer used for the SOI wafer is required originally for supporting an SOI layer via an insulator film; thus, no element is formed on the surface of the base wafer. Prior to the claimed invention herein and to reduce costs of a wafer, a wafer having COPs on its surface or a dummy-grade silicon wafer of which resistivity and the like do not

meet product standards had been used. That is, an epitaxial wafer and the like have never been used as a base wafer to be a support substrate even if they were used as a bond wafer to form an SOI layer (see page 5, lines 12-24 of the present specification). Nowhere does Inazuki teach or suggest detecting COPs existing in the base wafer as COPs existing in the SOI layer and that the insulator film and the base wafer could not be bonded in the region in which the COPs existed, resulting in a micro void. As such, Inazuki would not have led one to the present claims.

Therefore, Inazuki does not teach or suggest the use of an epitaxial wafer and the like as a base wafer, and claims 7 and 8 cannot be derived from Inazuki.

The Patent Office later acknowledges that Inazuki fails to use an epitaxial wafer and the like as a base wafer as claimed in the present application (see page 4, lines 1-4 of the Office Action).

The Patent Office turns to Abe as allegedly suggesting a similar method of manufacturing that includes the use of an FZ wafer as a base wafer. Applicant disagrees.

Abe relates to the use of an FZ wafer in accomplishing a decrease of signal transmission loss by using wafers of high resistivity as the base wafer. However, Abe only describes the so-called intrinsic gettering wafer, in which a CZ silicon wafer having a resistivity of 100 Ω·cm or more is subject to an oxygen precipitation heat treatment (see col. 9, lines 34-49), as a silicon wafer used for this base wafer of an SOI wafer besides the FZ wafer. Nowhere does Abe teach or suggest (1) detecting COPs existing in the base wafer as COPs existing in the SOI layer or (2) that the insulator film and the base wafer cannot be bonded in the region in which the COPs existed, resulting in a micro void. Thus, Abe does not teach or suggest using an epitaxial wafer, a nitrogen doped wafer, a hydrogen annealed wafer, a nitrogen doped and annealed wafer and an entire N-region wafer as wafers of which COPs are reduced for a base wafer.

The Patent Office further insists that Abe teaches a similar method of manufacturing that includes the use of an FZ wafer as a base wafer (see col. 11, lines 55-60). The Patent Office insists that it would have been obvious to one of ordinary skill in the art to substitute the base wafer of Inazuki with an FZ wafer because the advantage would allegedly be to create an SOI wafer with high resistivity against further semiconductor manufacturing processing.

However, as described above, Inazuki discloses using an epitaxial wafer or an FZ wafer as a bond wafer. Inazuki's effect is relevant to only cases where these wafers are used for a bond wafer. Therefore, Inazuki does not describe using these wafers as a base wafer at all. Namely, the invention described in Inazuki does not exhibit an effect until the epitaxial wafer or the FZ wafer is used as a bond wafer. On the other hand, as described above, the object of Abe is accomplishing a decrease of signal transmission loss by using an FZ wafer or the so-called intrinsic gettering wafer as wafers of high resistivity for a base wafer.

Thus, even if Inazuki and Abe were to have been combined as alleged by the Patent Office, the combination at best would have provided a method for producing an SOI wafer, wherein an epitaxial wafer or an FZ wafer as a silicon wafer of which COPs are reduced is only used for a bond wafer.

Therefore, amended claims 7 and 8 cannot be derived from the combination of Inazuki and Abe because the references do not teach or suggest using an epitaxial wafer, a nitrogen doped wafer, a hydrogen annealed wafer, a nitrogen doped and annealed wafer and an entire N-region wafer as wafers of which COPs are reduced, for a base wafer.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 7-22 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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